SET & SEU predictive tools

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Overview

- Heavy ion electrical model
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  - Bulk technology
  - FD SOI technology
- SET striker tool for analog IP
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- Digital libraries hardness characterization
  - Combinatorial and standard Flip-Flop
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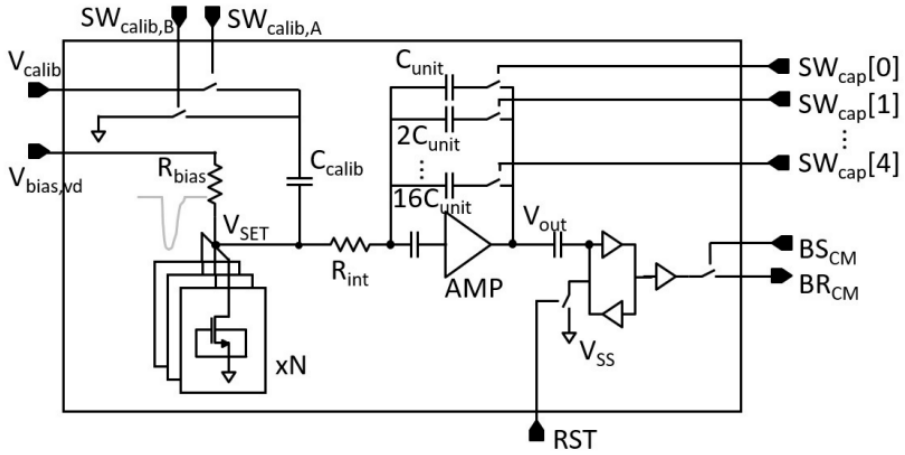
- Summary

Heavy ion electrical model

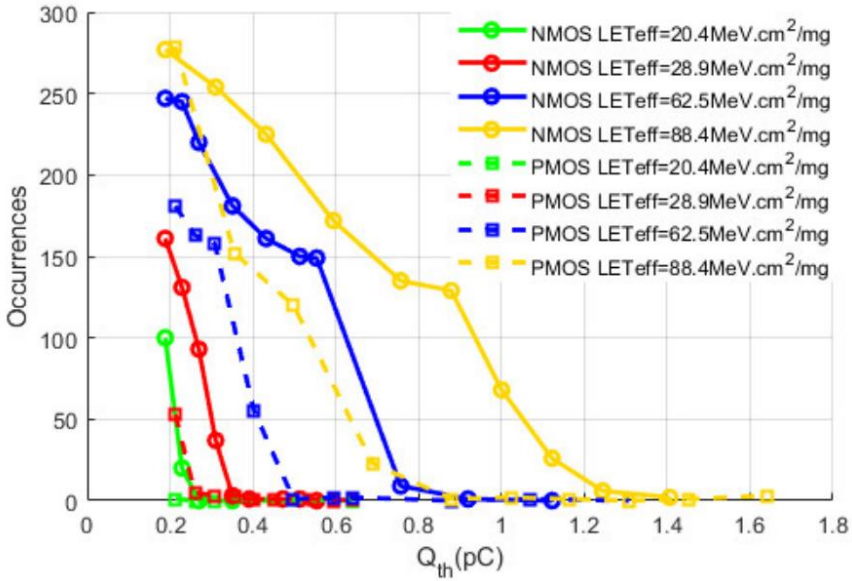
Test vehicle

[1] "Characterization of the Total Charge and Time Duration for Single-Event Transient Voltage Pulses in a 65-nm CMOS Technology", IEEE TNS 2022 vol.22 issue 7, Zheyi Li et al

- Goal is to make an electrical model of the heavy ion
  - Total charge collected and charge distribution [1]



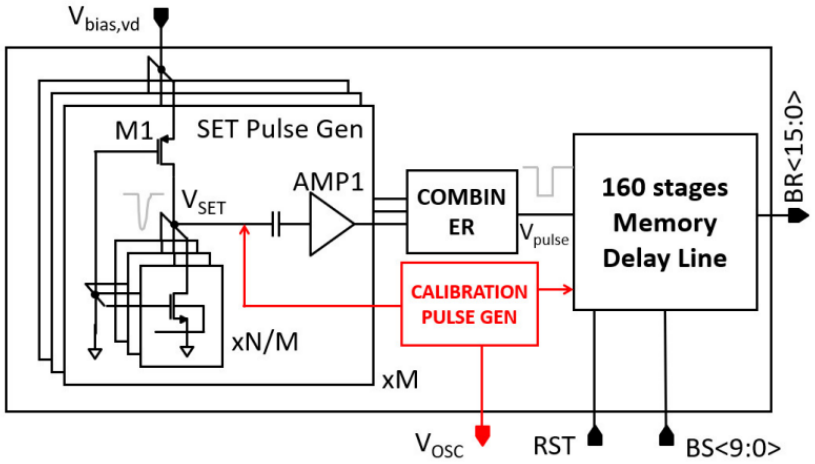
[1]



Heavy ion electrical model

Test vehicle

- Time constant, SET duration [1]



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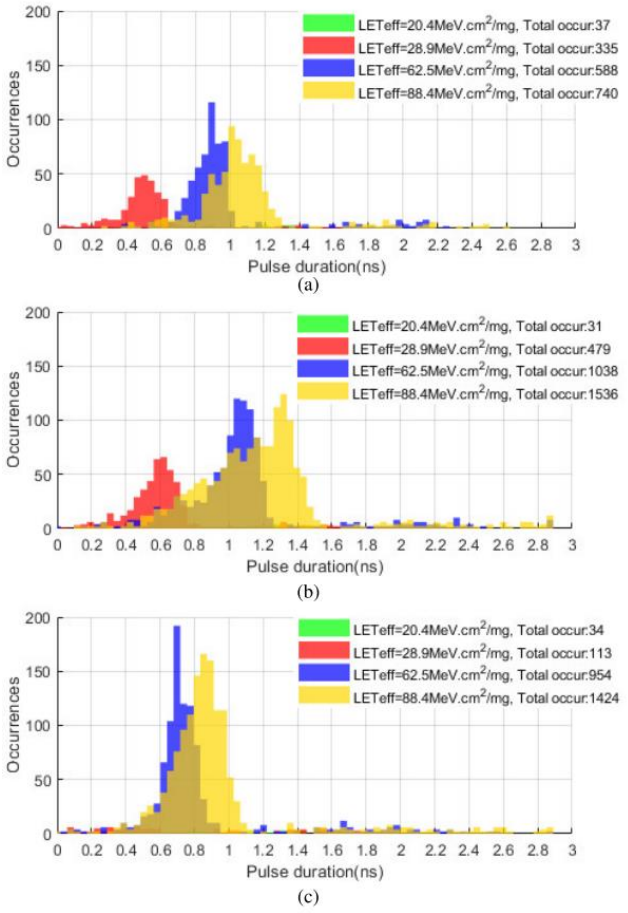


Heavy ion electrical model

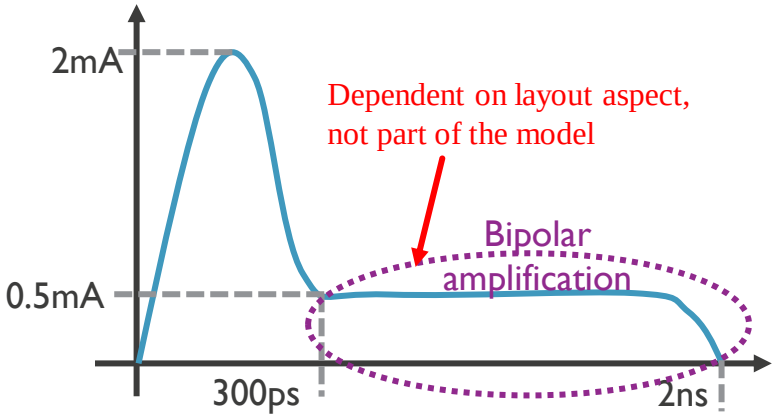
Bulk technology

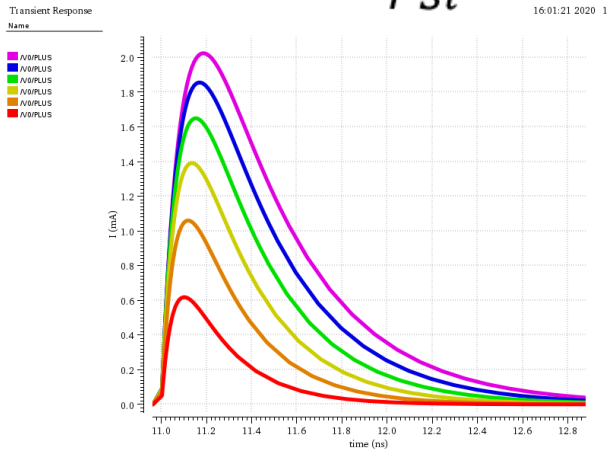
Model based on “double exponential” current pulse:
(ta = falling edge; tb = rising edge)

$$ISET = \frac{Q}{ta - tb}\left[e^{-\frac{t}{ta}} - e^{-\frac{t}{tb}}\right]$$

Linking LET and Q (collected charge):
(d = collection depth)

$$LET = \frac{Q \cdot 3{,}6eV}{e \cdot \rho_{Si} \cdot d}$$





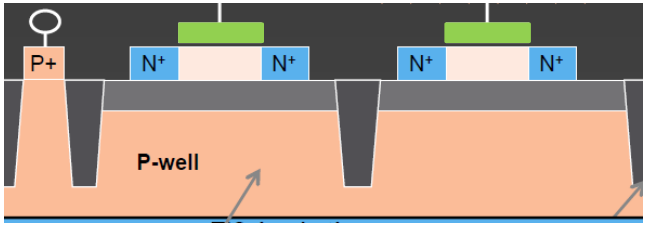
Heavy ion electrical model

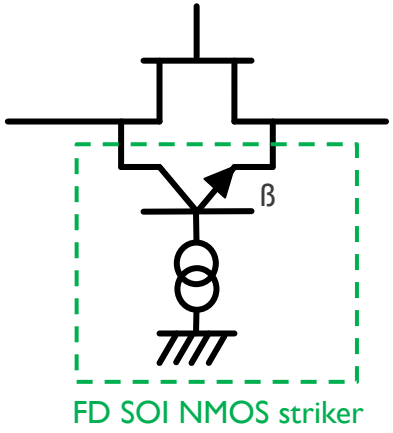
FD SOI technology

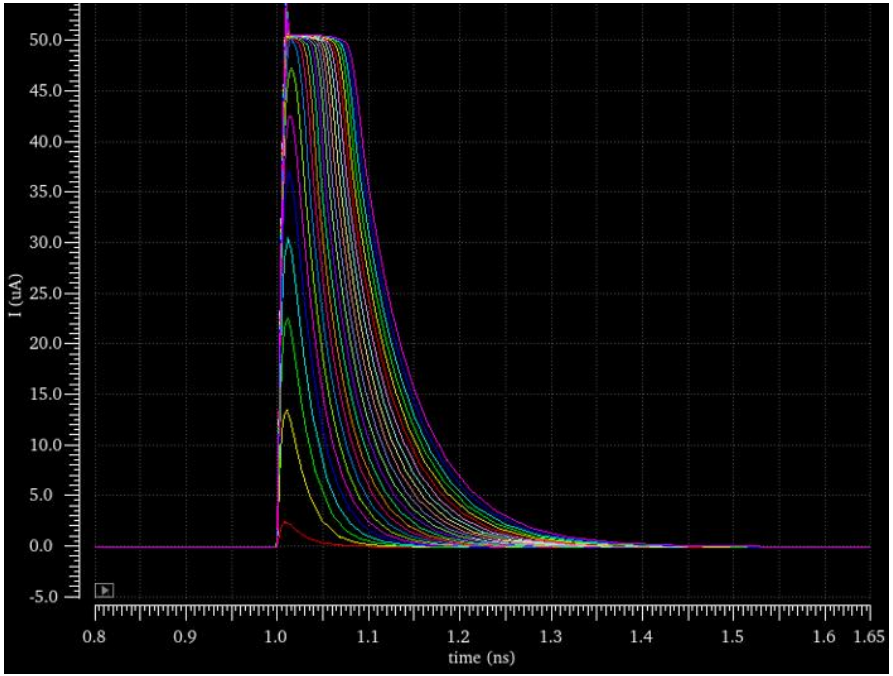
- The collected charge loads the silicon box and turns on the parasitic bipolar drain-box-source
- Electrical model based on parasitic bipolar with charge deposition on its base
- Collection depth is limited by the silicon thickness (order 5-20 nm)
- Model parameters:
  - Current gain of the parasitic bipolar
  - Collected charge
  - Time constant of the double exponential

Heavy ion electrical model

FD SOI technology







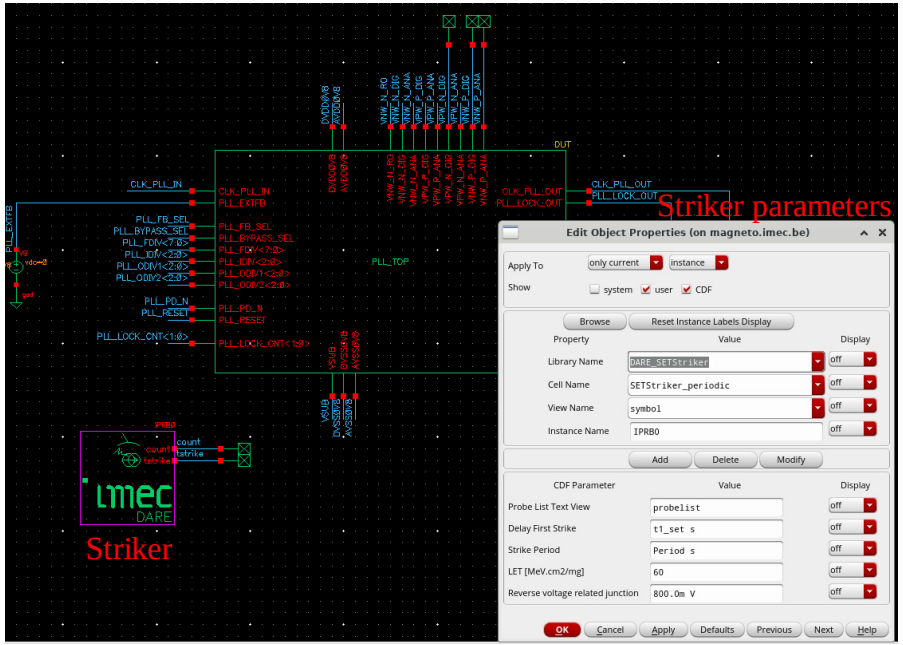
SET striker tool for analog IP

Description

- Electrical model of heavy ion strike implemented in veriloga
- Script to strike each transistor of the Device Under Test (DUT)
  - 1! transient simulation where each transistor is struck successively
  - Bulk: parallel junction filtered
  - FD SOI: parallel transistors filtered; bulk model used for diode & bulk transistor (ESD...)
  - Possibility to limit the analysis to fewer nodes selected by the designer

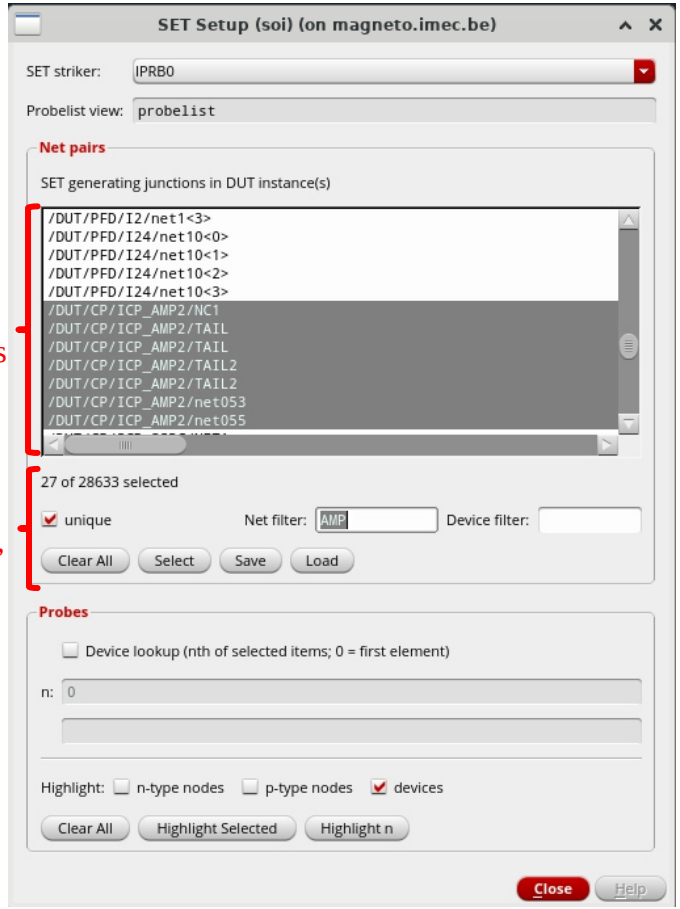
SET striker tool for analog IP

Description



List of DUT nets

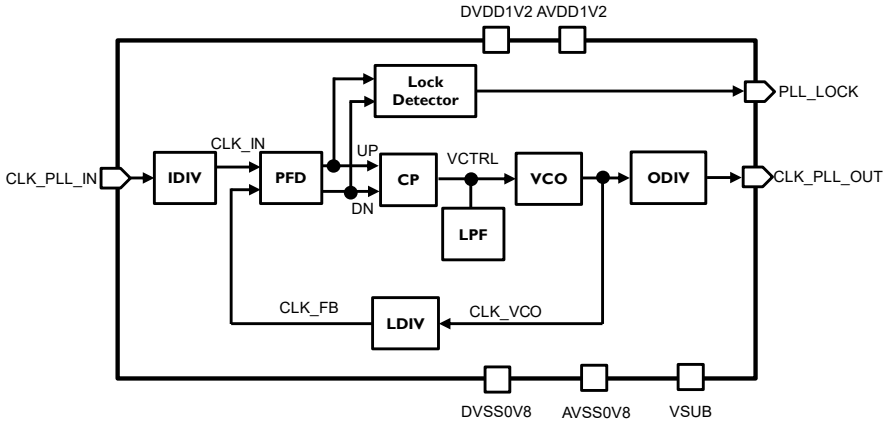
Filter based on net name, device name



SET striker tool for analog IP

Simulation versus measurement

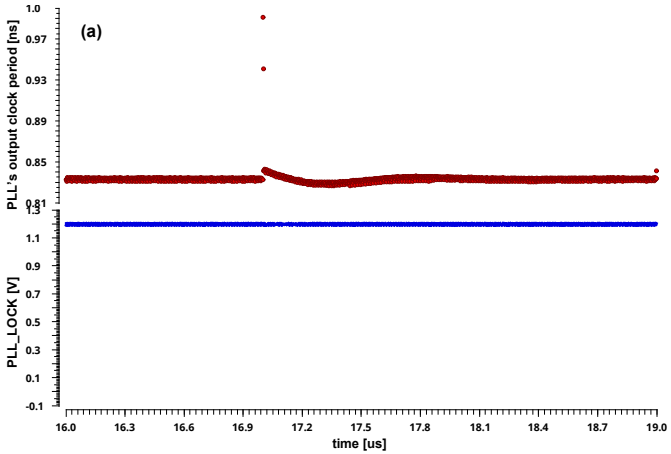
- PLL DARE65T
  - Each block (PFD, CP, VCO....) simulated separately
  - Complete PLL simulated with strike on VCO, Charge-Pump (CP) and bias current generator



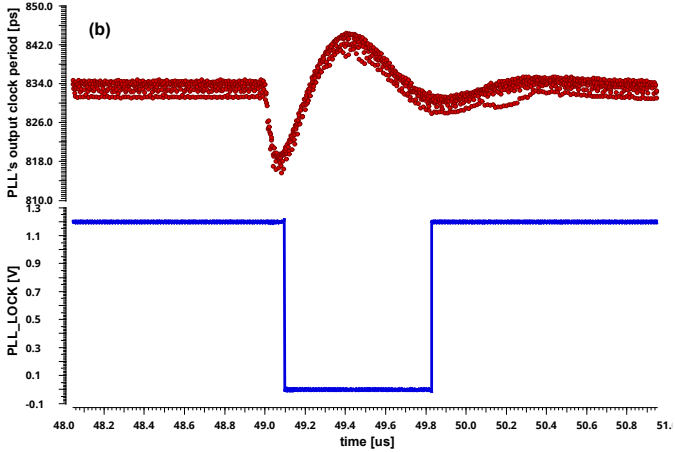
SET striker tool for analog IP

Simulation versus measurement

[2] “Single Event Effects Characterization Induced by Heavy Ions in 65-nm PLL”, RADECS 2022, SinNyoung Kim et al



Period jitter worst case 150ps (strike on VCO)



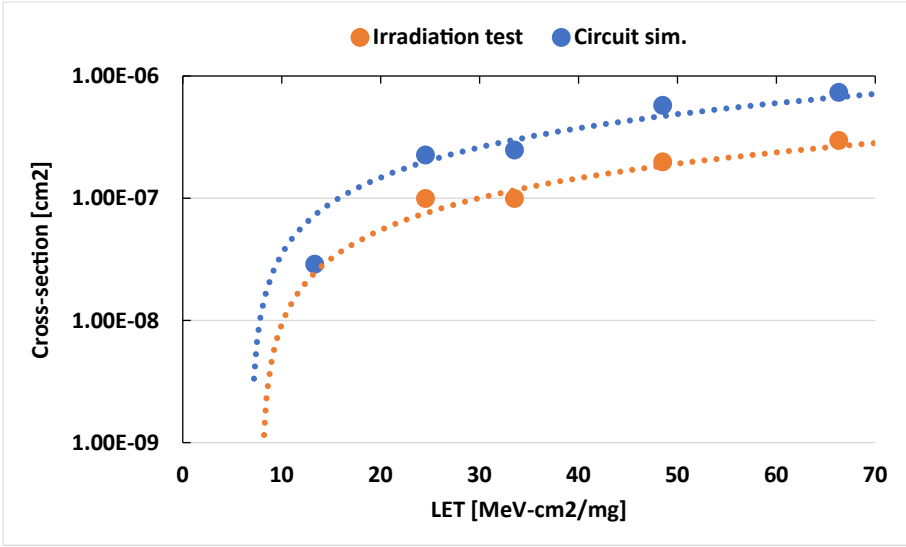
Accumulated jitter worst case (strike on Charge Pump)
Accumulated jitter lock criterium: phase shift > 2.2ns

SET striker tool for analog IP

Simulation versus measurement

[2] "Single Event Effects Characterization Induced by Heavy Ions in 65-nm PLL", RADECS 2022, SinNyoung Kim et al

	Simulation		Measurement	
LET [MeV-cm²/mg]	Cross-section [cm²]	Max. '0' level pulse width [us]	Cross-section [cm²]	Max. '0' level pulse width [us]
7	0	N/A	0	N/A
13	2.88×10^{-8}	0.5	0	N/A
24	2.25×10^{-7}	0.7	9.90×10^{-8}	0.6
33	2.47×10^{-7}	1.1	9.90×10^{-8}	0.6
48	5.74×10^{-7}	1.2	1.98×10^{-7}	0.7
66	7.32×10^{-7}	1.3	2.97×10^{-7}	1.6



Accumulated jitter cross-section (threshold 2.2 ns)

Digital libraries hardness characterization

Combinatorial cells and standard Flip-Flop

- Script to strike all transistors of the digital gate under test
  - Parallel simulation: 1! strike per simulation
  - Performed for different LET to detect the LET critical threshold of the gate under test
  - SET definition: propagation of the glitch through an inverter of minimum size connected to the gate under test output
  - Results concatenated in a single text file

Digital libraries hardness characterization

Dice Flip-Flop

- Script to strike each combination of 2 transistors of the DICE FF (simulate effect of a non-perpendicular strike)
  - Parallel simulation: 1! strike per simulation
  - Performed at max LET to detect transistor pair sensitive to double hit
  - Results concatenated in a single text file
- Goal: detect all the sensitive pairs (pairs of transistors leading to a SEU when simultaneously struck). Used to separate each transistor of a sensitive pair physically as far as possible from the other one

Summary

- Start from heavy ion strike model. Can come from:
  - Test vehicle measurement
  - Publication
  - Calibrated TCAD
- Home made tool to systematically strike all the nodes of the circuit
- Good matching between simulation and cyclotron measurement